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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of

SHIMAMOTO et al.

Application Number: 10/020,314

Filed: December 18, 2001

For: FABRICATING METHOD OF
SEMICONDUCTOR INTEGRATED CIRCUITS

Attorney Docket No. HTA-0143

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF NANCY DESANTI

Sir:

I, Nancy DeSanti, hereby declare the following:

- (1) I have been employed by Reed Smith LLP at the Falls Church Office located at 3110 Fairview Park Dr., Falls Church, Virginia 22043 since January 1997, and during that time I have been a Legal Secretary and an IP Secretary, and I have worked in the IP Division from September 1997 to the present.
- (2) Among my responsibilities, I am in charge of opening all incoming mail, including all Office Actions, Notices of Allowance and other communications issued by the U.S. Patent and Trademark Office (USPTO) in connection with all patents and patent applications being prosecuted, monitored or otherwise handled by our Falls Church IP Division office. I am also in charge of docketing all due dates associated with any such Office Actions, Notices of Allowances and other communications received from the USPTO.

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(3) Prior to the telephone call from the Examiner on September 20, 2005, in connection with the above-referenced application, our office had not received any communication from the USPTO after the Office Action mailed October 14, 2004 (to which a Response was filed January 6, 2005). Specifically, no Final Rejection was received. A copy of the docketing sheet is submitted herewith showing that no Office Action with a mailing date of March 23, 2005, was ever received and entered by our office. The only entry after the response of January 6, 2005, is for the receipt of the facsimile copy of the Office Action sent by Examiner Nguyen on November 4, 2005.

(4) I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-captioned application or any registration resulting therefrom.



Nancy DeSanti

Date: 2/26/06

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

United States Patent and Trademark Office																	
Home Site Index Search FAQ Glossary Guides Contracts eBusiness eBiz Alerts News Help																	
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10/020,314 Fabricating method of semiconductor integrat	
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Date 03-23-2005	Mail Final Rejection (PTOL - 32
01-27-2005	Date Forwarded to Examiner
01-08-2005	Workflow Incoming amendment
10-14-2004	Non-Final Rejection
08-13-2004	IFW TSS Processing by Tech C
08-03-2004	Request for Continued Examination
04-20-2004	Correspondence Address Change
01-06-2004	Mail Advisory Action (PTOL - 3
12-23-2003	Date Forwarded to Examiner
10-21-2003	Mail Final Rejection (PTOL - 32
08-28-2003	Date Forwarded to Examiner
05-06-2003	Mail Non-Final Rejection

HTA-0143USA		TITLE FABRICATING METHOD OF SEMICONDUCTOR INTEGRATED CIRCUITS												
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RELATED		STATUS	PENDING	ISSUE		18T	12/18/2001							
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AGENT														
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am	N	AMEND PUBLICATION	08/01/2002	21/M	10/01/2002		10/01/2002	0			1M	Y	YY	
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Advisory action mailed 1/8/04; RCE filed 1/16/04														
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(Waiting for official re-stmt date (copy of OA forced in advance))														
ASSIGNEES														
Renesas Technology Corporation														
INVENTORS														
SHIMAMOTO, Yasuhiro														
HIRATA, Masahiko														
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NABA-TAME, Toshihide														
ANDO, Toshiro														
SAKUMA, Hiroshi														
UJIMA, Shimpel														

USER-DEFINABLE FIELDS	
PUB#	
TXT2	
CASE	
P01432US00	ENTERED <input type="text" value="12/13/2001"/>
NOTES	<p>Jennifer Teng work stay case; Reassignment to Renesas Technology Corporation filed October 1, 2003; advisory action mailed 1/6/04; RCE filed 1/16/04; waiting for examiner to restart date (Office action dated 3/22/05 never received)</p>
SIMILAR CASES	
ART UNIT	
EXAMINER	
CONFIRM#	
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BY	
MODIFIED	<input type="text" value="01/31/2005"/>

HT#		HITA-0461 USA	
COUNTRY	US	UNITED STATES	
NEW/CON	NEW	SERIAL#	10460,155
RELATED		PATENT#	6,977,229
TYPE	UTL	STATUS	ISSUED
CLIENT	HITACHI		
AGENT			

TITLE									
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IF	N	ISSUE FEE	10/03/2005	1M		11/03/2005		11/03/2005	0
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M2	N	2ND MAINT FEE DUE	12/20/2005	80M		08/20/2013	16	12/20/2013	0
M3	N	3RD MAINT FEE DUE	12/20/2005	138M		08/20/2017	16	12/20/2017	0

INVENTORS

TOKOGAWA, Kenetku
IMOMONI, Yoshinori
IZAWA, Masaru

ASSIGNEES

Renesas Technology Corporation

PUB#	USER-DEFINABLE FIELDS	SMALL ENTITY	PATENT FIELDS
TXT2		CLAIMS	ART UNIT
CASE		PUBLICATION#	EXAMINER
			CONFIRM#
			SPF / ICM / IPFS
02/02/2006	ENTERED 06/10/2003 MODIFIED 12/21/2005 BY NDS	ATTORNEYS	

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<table border="1"> <thead> <tr> <th>Date</th> <th>Content</th> </tr> </thead> <tbody> <tr> <td>11-09-2005</td> <td>Mail Notice of Restarted Response</td> </tr> <tr> <td>03-23-2005</td> <td>Mail Final Rejection (PTOL - 32)</td> </tr> <tr> <td>02-03-2005</td> <td>Date Forwarded to Examiner</td> </tr> <tr> <td>01-21-2005</td> <td>Workflow Incoming amendment</td> </tr> <tr> <td>10-21-2004</td> <td>Non-Final Rejection</td> </tr> <tr> <td>09-15-2004</td> <td>Response to Election / Restriction</td> </tr> <tr> <td>08-24-2004</td> <td>Mail Restriction Requirement</td> </tr> <tr> <td>07-24-2003</td> <td>Reference capture on IDS</td> </tr> <tr> <td>07-24-2003</td> <td>Request for Foreign Priority (P)</td> </tr> <tr> <td>07-31-2004</td> <td>Case Docketed to Examiner in</td> </tr> <tr> <td>06-22-2004</td> <td>Application Return TO OIPE</td> </tr> <tr> <td>06-21-2004</td> <td>Application is Now Complete</td> </tr> </tbody> </table>		Date	Content	11-09-2005	Mail Notice of Restarted Response	03-23-2005	Mail Final Rejection (PTOL - 32)	02-03-2005	Date Forwarded to Examiner	01-21-2005	Workflow Incoming amendment	10-21-2004	Non-Final Rejection	09-15-2004	Response to Election / Restriction	08-24-2004	Mail Restriction Requirement	07-24-2003	Reference capture on IDS	07-24-2003	Request for Foreign Priority (P)	07-31-2004	Case Docketed to Examiner in	06-22-2004	Application Return TO OIPE	06-21-2004	Application is Now Complete
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06-21-2004	Application is Now Complete																										
																											

HTN	HITA-0415USA	
COUNTRY	US UNITED STATES	
NEWCON	SERIAL#	10/625,573
RELATED	PATENT#	
TYPE	UTL	STATUS PENDING
CLIENT	HITA	HITACHI
AGENT		

TITLE									
SEMICONDUCTOR MEMORY DEVICE									
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FR	N	FINAL REJECTION	11/09/2005	3M	02/09/2006	31	06/09/2006	0	1M YY YY

ASSIGNEES
HITACHI, LTD.

INVENTORS
SHAKAMOTO, Masatoshi
HASEGAWA, Masatoshi

USER-DEFINABLE FIELDS	ART UNIT
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TXT12	
CASE	
SMALL ENTITY	No
CLAIMS	
PUBLICATION#	
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ATTORNEYS	SPF / JCM / ISPT
ENTERED 07/09/2003	MODIFIED 01/30/2006 BY NDS

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FROM: REED SMITH LLP

FAX: 7032041352

TEL: 7036414547

COMMENT: CONFIDENTIAL

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